Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 91455

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2019
Sixth/Seventh/Eighth Semester
Electronics and Communication Engineering
EC 6601 – VLSI DESIGN
(Common to Electrical and Electronics Engineering, Biomedical Engineering, Electronics and Instrumentation Engineering, Medical Electronics, Robotics and Automation Engineering)
(Regulations 2013)
(Also Common to PTEC 6601 – VLSI Design for B.E. (Part-Time) Fifth Semester – Electronics and Communication Engineering and Third Semester – Electrical and Electronics Engineering – Regulations 2014)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Define threshold voltage of MOSFET.
2. Draw the stick diagram of NMOS NOR gate.
3. Compare static and dynamic power dissipation.
4. Draw a 2-input XNOR using NMOS pass transistor logic.
5. Compare latch and flip-flop.
6. Define set-up and hold time.
7. State the merits of barrel shifter.
8. Mention the different hardware architectures used for multiplier.
9. Compare full custom and semi-custom design.
10. State the building blocks of FPGA.

PART – B (5×13=65 Marks)

11. a) Highlight the need for scaling. Enumerate in detail constant electric field, constant voltage and combined electric field and voltage scaling for different parameters of MOSFET. (13)

(OR)

b) i) Derive an expression for rise time, fall time and propagation delay of CMOS invertor. (7)

ii) Derive the generalized expression for the propagation delay of N-cascaded CMOS inverters if 'N' is even and if 'N' is odd. (6)

12. a) i) Consider the given circuit Figure1. (9)

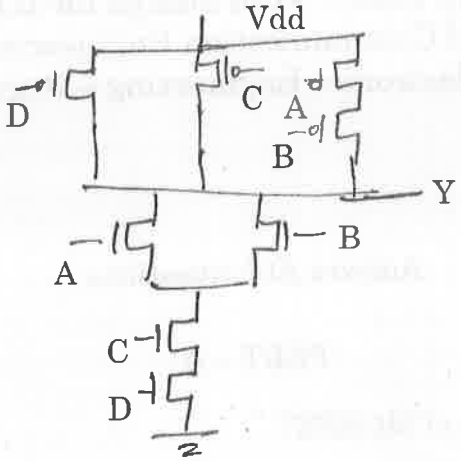

Figure1

What is the logic function implemented by the CMOS transistor network ? Size the NMOS and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS W/L = 4 and PMOS W/L = 8.

ii) Draw a static CMOS XOR gate. (4)

(OR)

b) i) State the different components of power dissipation in CMOS. Derive an expression for the dynamic power dissipation. (7)

ii) Implement the following expression in static CMOS logic fashion using no more than 10 transistors.

$Y = \overline{AB + ACE + DE + DCB}$. (6)

13. a) Realize a negative level sensitive latch using which realize an edge triggered master slave D-flip-flop. Explain its working. (13)

(OR)

b) Elucidate in detail the design of low power SRAM memory circuits. (13)

14. a) Design a 4-bit unsigned array multiplier. (13)

(OR)

b) i) Realize a 1-bit adder using static CMOS logic. (4)

ii) Optimize the Boolean expressions of sum and carryout and realize a 1-bit adder using static CMOS logic. (4)

iii) Also realize a 1-bit adder using transmission gate. Compare all the three cases from hardware perspective. (5)

15. a) Describe in detail FPGA architecture and explain the main building blocks of FPGA. (13)

(OR)

b) Give a note on standard cell design and FPGA interconnecting resources. (13)

PART – C **(1×15=15 Marks)**

16. a) i) Suppose we wish to implement the two logic functions given by F = A + B + C and G = A + B + C + D. Assume both true and complementary signals are available. Implement these functions in dynamic CMOS cascaded stages so as to minimize the transistor count. (8)

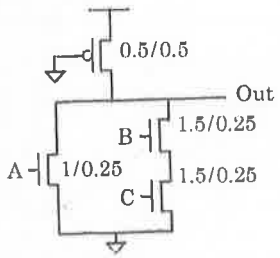

Figure 2

ii) What logic function does the circuit in Figure 2 implement ? To which logic family does the circuit belong ? Does the circuit have any advantages over fully complementary CMOS ? (7)

(OR)

b) i) With suitable example and with detailed steps explain Radix-4 modified booth encoding for an 8-bit signed multiplier. (8)

ii) Design a 4-bit barrel shifter. (7)